

ABSTRACT

High speed digital path for successive approximation analog-to-digital converters wherein the successive approximation registers and the switch drivers are combined in set-reset latches having the switch drivers as latch outputs. This reduces the time of each successive approximation by reducing the ripple through time of each stage, thereby increasing the speed of operation of the analog-to-digital converters. As an option, the set-reset latches having the switch drivers as latch outputs may also incorporate level shifting to combine each stage of the successive approximation register, associated switch drivers and level shifters into a single circuit for each stage of the analog-to-digital converter. Various embodiments are disclosed.